REMARKS

Claims 1 through 6 are pending. The abstract is also being amended.

Claims 1, 2, 3, 4, and 6 are being amended. The amendments are being made for clarity and not patentability purposes, and no new matter is being added.

Formal drawing replacements will be submitted at a later date.

In the Office Action, the Applicant has been reminded of the proper language and format for the abstract of the disclosure. In this respect, the Applicant has submitted herewith an amended abstract.

In the claims, an objection has been raised against the form of Claim 6 and so the amended claims submitted herewith also contain an amendment to Claim 6; it is now cast in independent form.

In response to the objections to FIGs. 2 and 3 raised in the Office Action, the drawings have been amended as shown in the attached corrected informal drawings to identify the voltage curves more clearly and correct a typographical error. Formal drawings as corrected, will be submitted subsequently.

Claims 2 through 4 stand rejected under 35 USC § 112 as failing to particularly point out subject matter which the Applicant regards as inventive. Claims 2 through 4 have now been amended to clarify that the non-linear characteristic recited in Claims 2 through 4 relates to capacitance.

Claims 1 and 6 are currently rejected under 35 USC § 103(a) as being obvious over US 5,287,241 (Puar) in view of US 6,667,870 (Segervall) and US 6,912,109 (Ker). Applicants are traversing this rejection.

The application presently contains two independent claims, namely Claims 1 and 6. Below, Applicants explain that the combination of Puar, Segervall and Ker do not disclose all of the elements of Claims 1 and 6.

Puar relates to a shunt circuit for electrostatic discharge protection. As explained in the abstract of this document, the shunt circuit is added to a Complementary Metal-Oxide Silicon (CMOS) Integrated Circuit (IC) to provide a non-reverse-biased shunt path between a power rail and a ground rail. According to col. 1, lines 47 through 57, input T1 of FIG. 4 is protected by diodes D1 and D2, the diodes being coupled to an inverter (P1, N1) via a resistor, R1. The actual protection circuit 400 comprises, according to col. 5, lines 6 through 13, a P-channel transistor P3, another P-channel transistor P4 and a capacitor C1. The capacitor C1 can be implemented as a P-channel or an N-channel transistor. Puar does not disclose connection configurations of bulks of any of the P-channel and/or N-channel transistors.

Claim 1 recites a circuit that is connected to an inverter of a clamp preamplifier. The circuit comprises a PMOSFET resistor having a gate connected to a ground rail, a drain connected to an input node of the inverter, and a source and a bulk connected to a power rail. The circuit also comprises an NMOSFET capacitor having a gate connected to the input node of the inverter. A drain, source and a bulk of the NMOSFET capacitor are coupled to the ground rail. Additionally, the circuit comprises a PMOSFET capacitor having a gate connected to the input node of the inverter, a drain and a source of the PMOSFET capacitor being connected to the ground rail. A bulk of the PMOSFET capacitor is connected to the power rail. As can be seen, each of the PMOSFET resistor, the NMOSFET capacitor and the PMOSFET capacitor is connected to the input node of the inverter.

As acknowledged in the Office Action, Puar does not teach the PMOSFET resistor (P4) having a drain connected to the input node of the inverted as recited in Claim 1. Puar teaches the PMOSFET resistor being coupled to the ground rail, the power rail and the P-channel clamping transistor (P3) / the capacitor (C1). Puar teaches the drain of the PMOSFET resistor (P4) being connected to the power rail. Puar does not teach the feature of an inverter of a clamp preamplifier as recited in Claim 1. Puar teaches the inverter (P1, N1) and the clamping transistor (P3) as being distinct. Puar does not disclose the gate of the NMOSFET capacitor being connected to the input node of the inverter as recited in Claim 1. The connection of the gate of the NMOSFET capacitor is not specifically disclosed in Puar and the reader is left to choose between a connection to the ground rail and the source of the PMOSFET resistor (P4) / the gate of the clamping transistor (P3), but definitely not the input node of the inverter. As acknowledged in the Office Action, Puar does not disclose the

PMOSFET capacitor or the preamplifier and recited in Claim 1 and acknowledges that the clamping transistor is not the same as a preamplifier.

The Office Action firstly relies upon Sergervall to disclose an additional capacitor. Sergervall also relates to an electrostatic discharge protection circuit. As shown in FIGs. 2 and 5, the circuit comprises an inverter (M2/M3 in FIG. 2 and M0/M1 in FIG. 5). The capacitor (C3) has a bulk that, as shown in FIG. 5, is floating. The bulks of other FET capacitors (C1, C2) are, in contrast, connected to the ground rail.

Sergervall fails to disclose the PMOSFET capacitor having a gate connected to an input of the inverter as recited in Claim 1. Further, Sergervall does not teach the bulk of the PMOSFET capacitor being connected the power rail as recited in Claim 1. The bulk of the capacitor (C3) of Sergervall is neither connected to the power rail or the ground rail. Sergervall also fails to disclose the connection details of the PMOSFET resistor and the NMOSFET capacitor as recited in Claim 1.

Reliance is therefore further placed upon the teachings of Ker. Ker also relates to an electrostatic discharge protection circuit. FIG. 12 of Ker discloses an inverter (28, 30) having an input node connected to a gate of an FET 48 serving as a capacitor. Only a single capacitor is disclosed in FIG. 12. Whilst FIG. 11 discloses a further transistor 44, the further transistor 44 serves as a gate oxide protection transistor. FIG. 12 discloses a resistor (12) coupled between the input node of the inverter and the ground rail. According to col. 9, lines 48 through 50, the resistor R can be implemented as "a poly resistor, a diffusions resistor or a well resistor".

Ker does not teach a PMOSFET capacitor having a drain and a source connected to the ground rail as recited in Claim 1. Further, Ker does not teach a PMOSFET resistor as recited in Claim 1. The resistor of Ker is formed as a poly resistor, a diffusion resistor or a well resistor. Ker also does not teach the NMOSFET capacitor as recited in Claim 1.

A combination of the teachings of Puar, Sergervall and Ker does not teach the skilled person to arrive at the combination of features as recited in Claim 1. In particular, the combined teaching fails to teach a PMOSFET resistor having a drain connected to an input node of the inverter as recited in Claim 1. The combined teaching only discloses a possible use of a poly resistor, a diffusion resistor or a well resistor.

In addition to the above combination of documents, the Office Action additionally proposes a modification (that is believed to be obvious to one of ordinary skill) to the transistor 48 of Ker (FIG. 12) to make the transistor 48 read onto Claim 1. Hence, to arrive at a conclusion of obviousness, the Office Action has put forward a combination of three documents plus a further modification of one of the documents alleged to be obvious to one of ordinary skill. It is therefore respectfully submitted that an impermissible degree of hindsight, contrary to the guidance of the MPEP, is being employed. This is particularly apparent, since the modification to the connections of the transistor 48 that is deemed obvious to one of ordinary skill is being suggested in the Office Action without reference to evidence in the cited prior art to suggest a motivation to make such a modification. Therefore, it is submitted that the combination of the teachings of Puar, Sergervall and Ker involve an impermissible degree of hindsight.

In view of the reasoning provided above, Applicants submit that the combined teachings of the Puar, Segervall and Ker documents cannot be combined, and even if combined, do not render Claim 1 obvious.

Claims 2 through 5 depend from Claim 1. By virtue of this dependence, Claims 2 through 5 are also not rendered obvious.

Claim 6 corresponds to Claim 1 and so the arguments submitted above in support of Claim 1 also apply to Claim 6 and so the combined teachings of the Puar, Segervall and Ker documents do not render Claim 6 obvious.

Respectfully submitted,

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